CLEAN ROOM

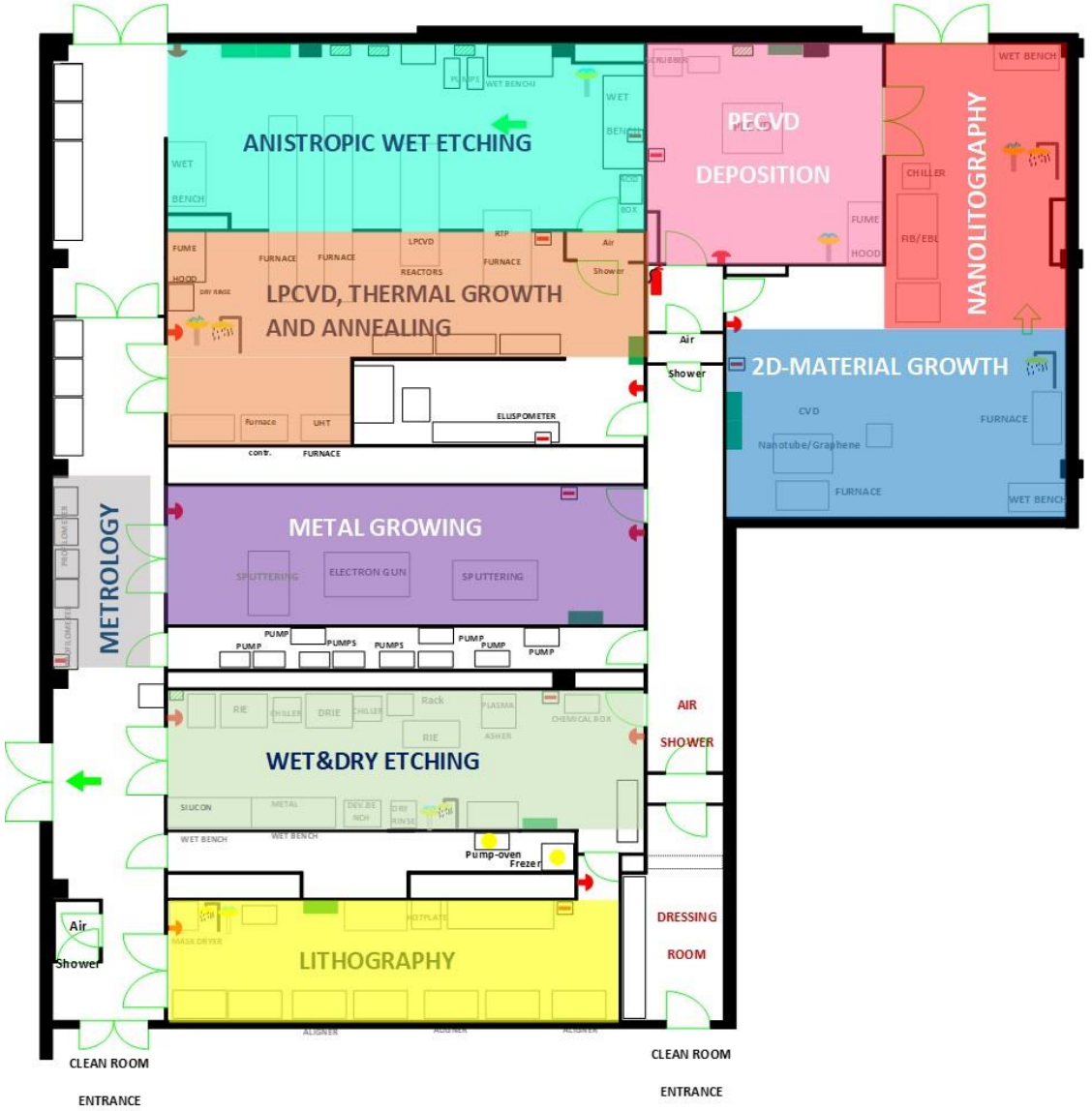
- 500 m^2, ISO 5-8
- 100 mm (4”) Wafer line
- Devices, materials and processes for
  - ✓ Microelectronics
  - ✓ Sensors and microsystems
  - ✓ Photovoltaic and optoelectronic devices
  - ✓ Gaphene technology

CLEAN ROOM LAYOUT

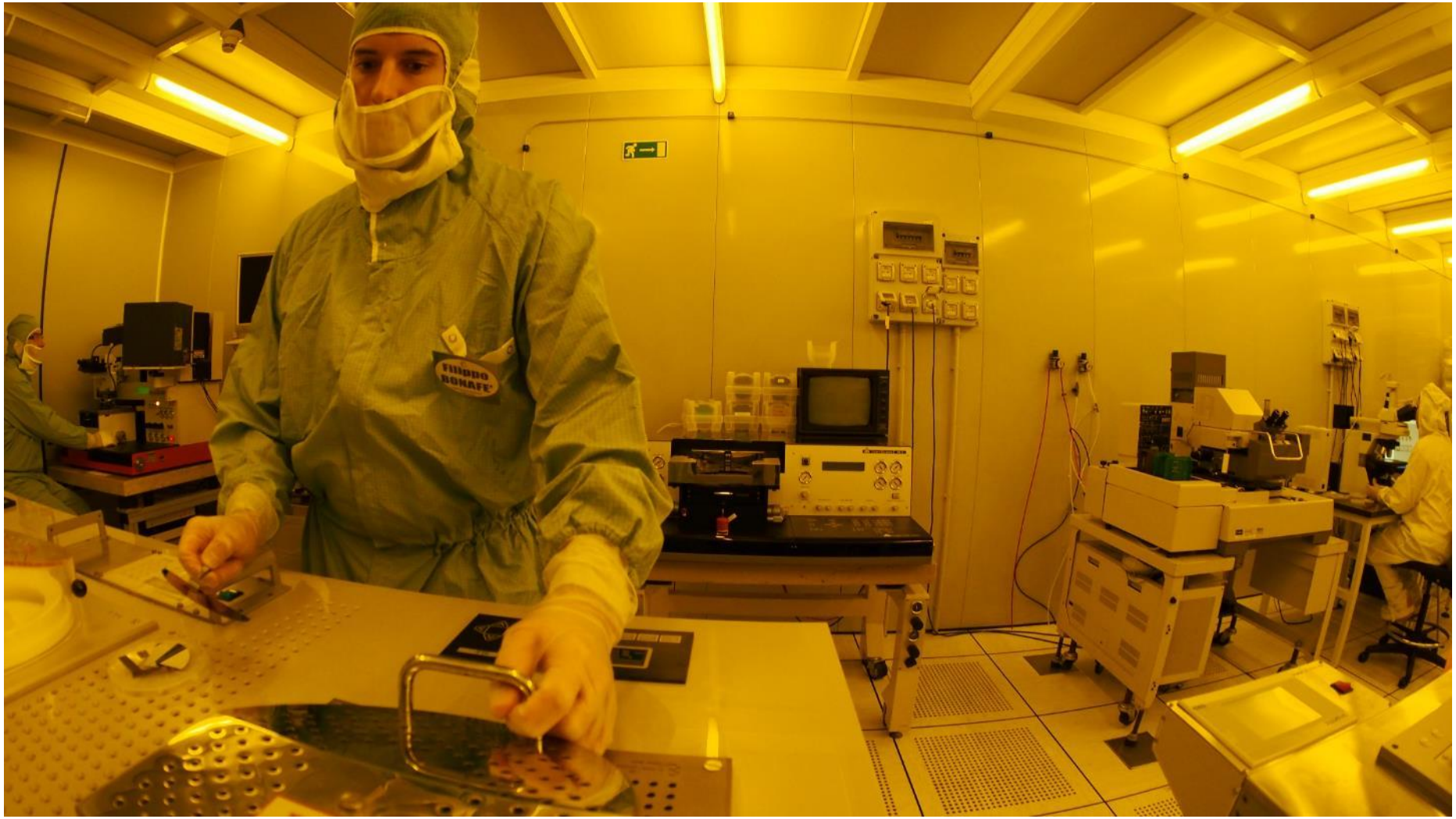
CLEAN-ROOM FACILITIES

- Si and SiC thermal processes
- LPCVD and multichamber PECVD reactors
- Hot-wall and cold-wall CVD reactors
- Sputtering and evaporators
- Reactive Ion Etchers (RIE) and Deep RIE for Si and Silicon oxide
- Medium and high energy ion implanters
- Rapid Thermal Process systems
- Front and front-to-back side mask aligner
- Soft nanoimprint system and replication tools
- Wet anisotropic silicon etching (KOH, TMAH)
- Wafer bonder (anodic, fusion, SU-8, and glass frit)
- Wafer dicing and wire bonding system
- ZEISS CrossBeam 340 FIB/SEM with Raith EBL

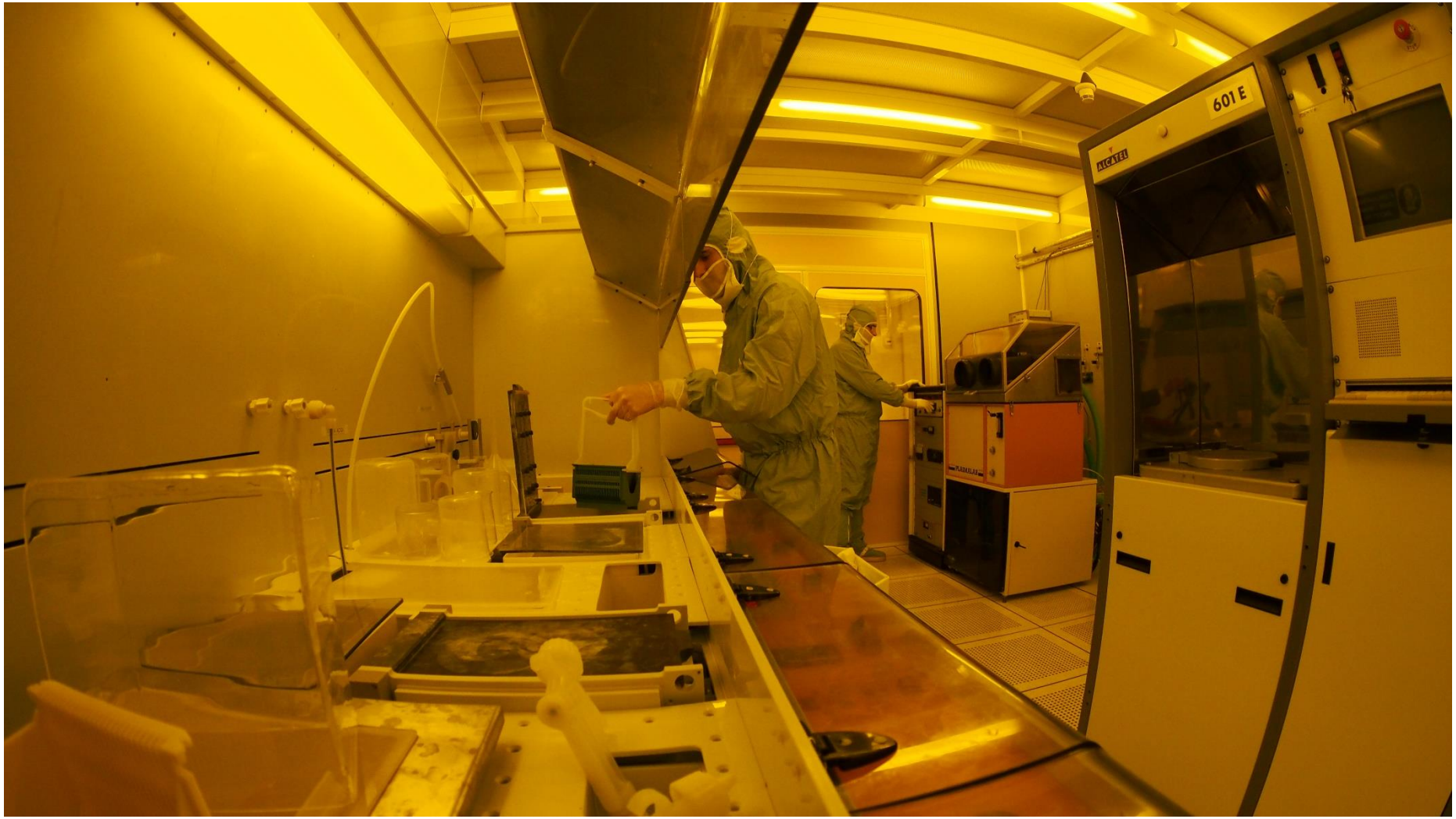
500 m² (250 m² ISO 5) MEMS and CMOS Clean-Room



CLEAN ROOM - LITHOGRAPHY



CLEAN ROOM – WET AND DRY ETCHING



CLEAN ROOM – METAL DEPOSITION

CLEAN ROOM – GROWTH AND ANNEALING

CLEAN ROOM – PECVD DEPOSITION

CLEAN ROOM – GRAPHENE GROWTH

CLEAN ROOM – NANOLITHOGRAPHY